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Implementation of Charge Leakage and Sharing Noise Susceptible Dynamic CMOS Design

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Abstract

Noise issues are becoming a main concern in digital systems due to the aggressive scaling trends in devices and interconnections. In this paper, we proposed a PMOS and NMOS keeper logic to improve the voltage transitions in dynamic gates. This keeper circuit technique is proposed in this paper for simultaneous power reduction and speed enhancement of dynamic logic circuits. The threshold voltage of the keeper transistor is modified during circuit operation to reduce the contention current without sacrificing noise immunity.

Keywords: Noise Susceptible, CMOS Design.

Introduction

Dynamic CMOS logic is also called as precharge evaluate logic. It allows to significantly reducing the number of transistors used to implement any logic function. The circuit operation is based on first percharging the output capacitance and subsequently, evaluating the output level according to the applied input. Both of these operations are scheduled by a single clock signal, which drives one NMOS and one PMOS transistor in each dynamic stage Fig 1 shows the CMOS dynamic logic NOR gate implemented using dynamic logic. It consists of pull down network structure whose output node is precharge to VDD by a PMOSFET and conditionally discharge by NMOSFET connected to VSS. The precharge phase occurs when clk=0. The path to the VSS supply is closed via the NMOS during clk=1 (evaluate phase). The pull up time is improved by PMOSFET, but the pull down time is increased due to the ground switch (NMOS).

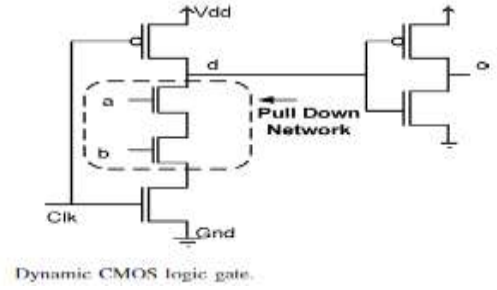

Fig 1 Dynamic cmos logic gate

The number of problem arises in this structure firstly, the inputs can only change during the precharge phase and must be stable during the evaluate portion of the cycle. If this condition is not met, charge redistribution effects can corrupt the output node voltage. Secondly the multistage application of dynamic logic presents a significant problem. For instance consider the two stage cascaded structure. Here the output of first dynamic CMOS stage drives one of the inputs of the second dynamic CMOS stage, which is assume to be two input NAND gate for simplicity. Fig 2 shows Cascade connected Dynamic NOR Logic.

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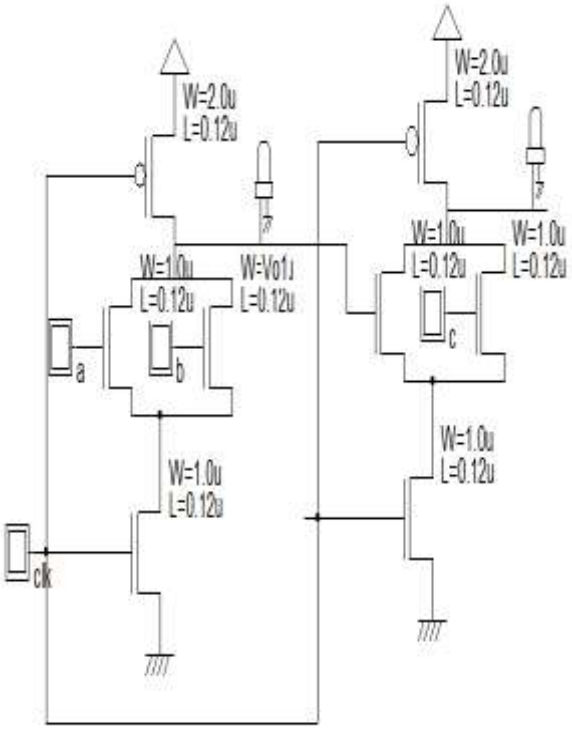

Fig 2 Cascade connected Dynamic NOR Logic

During the precharge phase both output VO1 and VO2 are pulled up by the respective PMOS precharge devise. Also the external inputs are applied during this stage. During the evaluate phase, the output of the first gate will conditionally discharge. However some delay will be incurred due to finite pull down time. Since the evaluation in the second stage is done concurrently, VO1 can discharge to VSS but the output voltage VO2 t the end of the evaluation phase will be erroneously low. Fig 3 shows Timing simulation of cascaded dynamic NOR logic The correction of this stage is not possible. Thus the clocking schemes and circuits structure must be develop to overcome this problem.

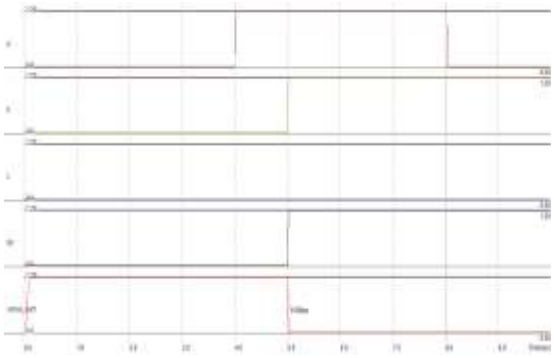

Fig 3 Timing simulation of cascaded dynamic NOR logic

The drawback arises in cascaded dynamic logic is avoid by incorporating a static CMOS inverter into each dynamic logic gate as shown in Fig 4 .The addition of the inverter allows us to operate a number of such structure in cascade. During precharge (clock =0), the output of first stage of the dynamic gate is precharge high and the output inverter is low. As subsequent logic stages are fed from thin inverter, transistor of second stage will be turned off, during the precharge phase. The evaluation phase, there may cause the output node of the dynamic CMOS stage (first stage) is either discharge to a low level through the PDN (1 to 0 transition) or it remains high. Consequently, the inverter output voltage can also make at most one transition during the evaluation phase from 0 to 1. In cascade structure consisting of several such stages, the evaluation of each stage ripples the next stage evaluation, similar to a chain of domino's falling one after another. The structure is hence called domino CMOS logic.

There are some other limitations associated with domino CMOS logic gates. The additional capacitance at each node of the series connected MOS logic makes speed slow and may cause charge redistribution which results in noisy output. This will be explaining in the following.

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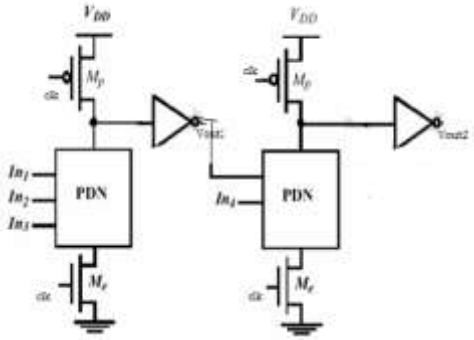

Fig 4 Domino logic

Domino CMOS logic

Consider the domino CMOS logic shown in Fig 5 Charge sharing between capacitors We will assume that all inputs are low initially, and the load voltages across C2 to C5 are zero volts. During the precharge phase, the output capacitance C1 charged up to its logic high level of VDD through PMOS transistor. During evaluation phase, if we assume that input A0 is low and inputs A0 toA3 are high. The charge stored in output capacitance C1 will now be shared iby C2, leading to so called charge-sharing phenomenon. The output node voltage after sharing between C1 and C2 becomes VDD/(1+C1/C2). For example, if C1=C2, the output voltage becomes VDD/2 in the evaluation phase. Depending on the ratio of the capacitance, this level could erroneously go low. Thus output voltage of the following inverter will then switch high, which is a logic error. Several measure can be taken in order to prevent erroneous output levels due to charge sharing in domino CMOS gate. It is done by precharging the internal pull down network node along with the precharge node itself, although at the cost of area and

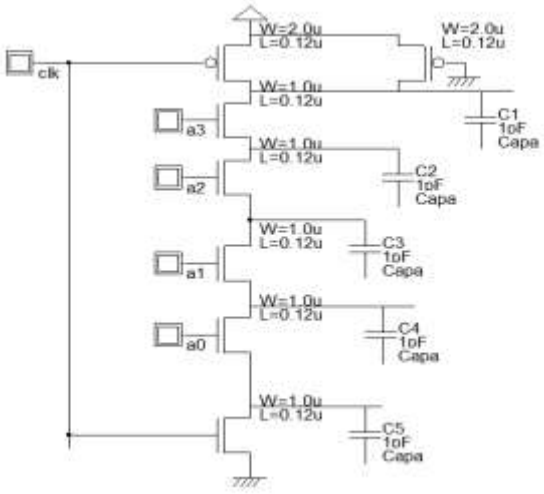

Fig 5 Charge sharing between capacitors

complexity. It uses a weak PMOS pull up device (with a small W/L ratio) to the dynamic CMOS stage output, which essentially forces a high output level unless there is a strong pull down path between the output and ground. The weak PMOS will turn on only when the precharge node voltage is VDD, otherwise it will turn off.

Another problem is Charge leakage problem which is caused mainly because of leakage current causes by minority charge carriers, as shown in figure 6. Charge sharing and charge leakage are unwanted elements in a circuit ,which causes unwanted voltage transition termed as Noise.

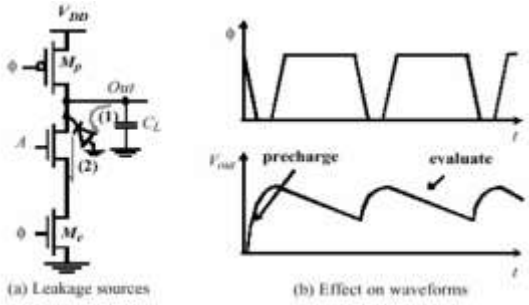

Fig 6 Charge leakage

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Proposed Stack method to reduce noise

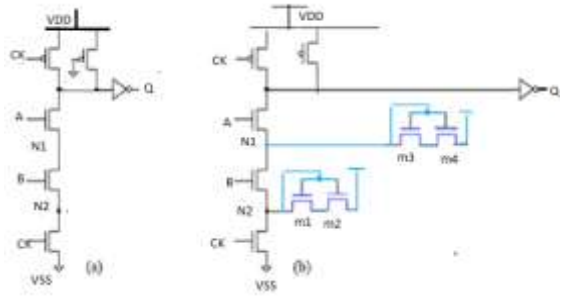

Fig 7 Dynamic cmos Nand gate using stack transistors

Stack method to reduce Noise

Charge leakage problems are reduced to a certain extent , by using stack of transistors rather than a single transistor. As shown in figure 7 (b) , a dynamic cmos logic Nand gate with a pmos keeper is shown in figure (a), it would have noisy effects because of charge leakage problem, so in order to make it Noise free NMOS keeper circuits are employed to its node N1 and N2 as shown in figure 7 (b) implementation of both the layouts is shown in figure 8, and simulation is shown in figure 9.

Fig 8 layout of Dynamic cmos Nand gate using stack transistors

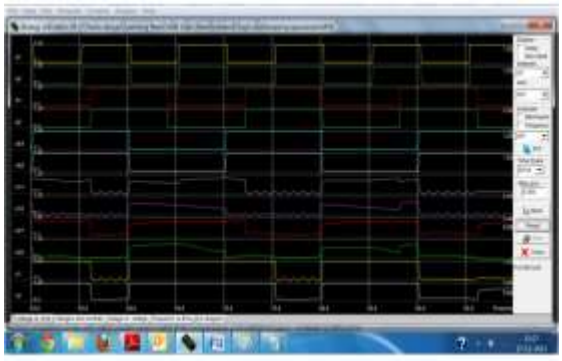

Fig 9 simulation of Dynamic cmos Nand gate using stack transistor

Parametric analysis

Comparative study of past and proposed method

Cell	Pre optimize Number of transistor	Post optimize Number of transistor	Pre optimize Maximum Ids mA	Post optimize Maximum Ids mA	Pre optimise Noise V	Post optimise Noise V
source voltage at node With NMOS	7	9	0.426	0.475	0.2	0.04
source voltage at node With PMOS	7	9	0.261	0.353	0.2	0.03
Feedback keeper	6	8	0.374	0.509	0.2	0.04
Precharge all internal nodes	7	9	0.432	0.573	0.2	0.03
Propose logic layout	7	11	0.432	0.616	0.2	0.02

Conclusion

In this paper, we proposed stack of transistors as a keeper rather than single transistor . Stack of transistor or stack transistors reduces charge leakage and thus provides the noise immunity to the circuit. And thus soft errors protection can be done, Noise of the device is also determined and reduced ,Performance of the CMOS is improved output current has been enhanced. .In this paper, we presented an analytical model for keeper transistor sizing to meet the noise constraint. Simulation results show that our analytical model can be applied effectively to Nand gate ,.

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